# Application Note 191

Toolchain Extensions for R8051XC/R8051XC2 Core

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This Application Note tells you how to configure the Keil 8051 development tools for Evatronix R8051XC/R8051XC2 based devices. The R8051XC/R8051XC2 is a highly configurable IP core that provides many extensions such as configurable DPTR registers, MDU, and a flexible set of peripherals.

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## Overview

This application note describes the configuration features for the  **Evatronix R8051XC/R8051XC2** CPU core that are available in the  **Keil PK51 Professional Developer's Kit**.

* The **�Vision� Device Database�** allows to define new devices that you have created with the **R8051XC/R8051XC2** CPU core. Refer to the article [UVISION: ADDING CUSTOM PARTS TO THE DEVICE DATABASE](http://www.keil.com/support/docs/1421.htm) for information on how to create a new device within the �Vision environment. The article [UVISION: ADDING A USER-SPECIFIC DEVICE DATABASE (CDB FILE)](http://www.keil.com/support/docs/1645.htm) explains how to organize new devices in a custom device database.
* The **�Vision Simulation DLLs** can be configured to cover several aspects of the **R8051XC/R8051XC2** CPU core.
* The standard **code banking** feature of **Keil PK51** allows you to use the program memory banking feature of the **R8051XC/R8051XC2** CPU core
* The **Keil C51 Compiler** provides extensions to use the multiple DPTR registers and the MDU of the **R8051XC/R8051XC2** CPU core.

**NOTE:**

* The  **R8051XC** extensions described in this application note are part of Keil PK51 Version 8.03 or higher. Previous versions do not support the R8051XC features.
* The **R8051XC2** extensions are part of Keil PK51 Version 8.19 or higher.

## Device Database Configuration

The **�Vision Device Database** allows you to create custom devices that simplifies the configuration tool configuration. The article [UVISION: ADDING CUSTOM PARTS TO THE DEVICE DATABASE](http://www.keil.com/support/docs/1421.htm) explains the various configuration options.

The string **CPU=** configures the memory sizes of the device and specific options such as MDU or multiple DPTR. The following options are relevant for the **R8051XC/R8051XC2**:

* **MODC2**: enable 2 DPTR registers in both the simulator and the C51 Compiler. For more information refer to the **C51 User's Guide - MODC2 Compiler Directive.**
* **MOD517DP**: enable 8 DPTR registers in both the simulator and the C51 Compiler. For more information refer to the **C51 User's Guide - MOD517 Compiler Directive.**
* **MDU\_R515**: configure for Multiply/Devide Unit of Evatronix R8051XC. Allows you to use the C51 extensions for MDU. For more information refer to the **C51 User's Guide - MDU\_R515 Compiler Directive.**

The string **SIM=** configures the CPU and Peripheral simulation DLLs. For the R8051XC/R8051XC2 device you need to use the DLL's **S8051.DLL** and **DCore51.DLL** with the parameter -**pR8051XC** or **-pR8051XC2**. Additional parameters are described in the next section [Simulator Configuration](#_3znysh7).

**Sample configuration options:**

CPU=IRAM(0-0x7F) CLOCK(12000000) MOD517DP MDU\_R515  
SIM=S8051.DLL("-PMW -DPC -BSE") DCore51.DLL("-pR8051XC")

## Multiple DPTR Support

The R8051XC/R8051XC2 device provides auto-increment features and automatic saving of the multiple DPTR register banks. When using the C51 directive BSE, the compiler does no longer save the DPTR registers when switching register banks. When using this feature together with the MOD517 directive, the C51 Compiler uses the auto-increment features with the C51 library functions **memcpy**, **memcmp**, **memmove**, **strcpy**, and **strcmp**.

## Simulator Configuration

The R8051XC/R8051XC2 device is simulated with the CPU DLL **S8051.DLL** and the Dialog DLL **DCore51.DLL**. These DLL provide several parameters that provide configuration features for the device. The parameters may be entered in the �Vision dialog page **Options for Target - Debug**. When you select a device from the device database, the DLL parameters are copied from the string **SIM=** as described in the previous section [Device Database Configuration](#_30j0zll).

### **S8051.DLL Parameters for R8051XC**

* **-PMW**: enable the PCON.PMW feature that allows to use MOVX instructions to write into the code space.
* **-DPC**: enable the data pointer control registers that provide auto-increment features for the DPTR registers.
* **-BSE**: enable the Bank Switch Enable feature in the register DPSEL.3.
* **-XB 95**: enable xdata banking register D\_PAGESEL at SFR address 0x95 (the SFR address is configurable).

### **DCore51.DLL Parameters for R8051XC**

* **-pR8051XC**: configure for the R8051XC core.
* **-pR8051XC2**: configure for the R8051XC2 core.
* -**oXXXXXXXXX**: specifies the implemented peripherals. XXXXXXXX is a 64-bit HEX number that is encoded as shown table below:

| * Bit | * Description |
| --- | --- |
| * 0 | * Port 0 |
| * 1 | * Port 1 |
| * 2 | * Port 2 |
| * 3 | * Port 3 |
| * 4 | * Timer 0 |
| * 5 | * Timer 1 |
| * 6 | * Timer 2 |
| * 7 | * UART 0 |
| * 8 | * UART1 |
| * 9 | * PMU (Power Management Unit) |
| * 10 | * PMW (Program Memory Write) |
| * 11 | * MDU (Multiplication/Division Unit) |
| * 12 | * CKCON (Clock Control) |
| * 13 | * Watchdog |
| * 15-14 | * 00: No Interrupt Controller 01: 8051 compatible, 2-level 10: 80515 compatible, 4 level 11: invalid |
| * 17-16 | * 00: no DPTR 01: one DPTR 10: two DPTR (implies device database string **CPU=MODC2)** 11: eight DPTR  (implies device database string **CPU=MOD517DP)** |
| * 18 | * DPTR auto increment |
| * 19 | * I2C |
| * 20 | * SPI |
| * 24-21 | * 0000: no external interrupt 0001: 1 external interrupt 0010: 2 external interrupts 0011: 3 external interrupts : 1100: 12 external interrupts 1101: 13 external interrupts |
| * 25 | * Disable MUL instruction |
| * 26 | * Disable DIV instruction |
| * 27 | * Disable DA instruction |
| * 30-28 | * 000: no additional address lines (16 bit address, no code banking) 001: 1 additional address line 010: 2 additional address line : 111: 7 additional address line |
| * 31 | * Second I2C |
| * 32-35 | * Prescaler width for extended watchdog timer 0000: no additional prescaler (standard watchdog timer) 0001: 1-bit prescaler (divide by 2) 0010: 2-bit prescaler (divide by 4) 0011: 3-bit prescaler (divide by 8)     :          : 0111: 7-bit prescaler (divide by 128) 1000: 8-bit prescaler (divide by 256) other values are reserved |
| * 36-39 | * Number of DMA channels 0000: DMA controller disabled 0001: 1 DMA channel 0010: 2 DMA channel     :          : 0111: 7 DMA channel 1000: 8 DMA channel other values are reserved |
| * 40 | * Software Reset |
| * 41 | * RTC (Real Time Clock) |
| * 42-63 | * unused |



Configuration parameter examples for the DCore51.DLL:

* **-pR8051XC2 -o38081BFBFFF (default)**: enables port 0-3, timer 0/1/2, UART 0/1, PMU, PMW, MUL/DIV, CKCON, Watchdog timer, ISR515, eight DPTR, DPTR auto increment, I2C, SPI, 13 external interrupts, full instruction set, no additional address lines. second I2C, no watchdog prescaler, 8 DMA channels, software reset, RTC.

**NOTE:**

* The peripheral simulation components of the DCore51.DLL may be expanded by using the AGSI Interface. Refer to  [Application Note 154: Implementing DLLs for User-defined Simulation (AGSI)](http://www.keil.com/appnotes/docs/apnt_154.asp) for more information.

### **Evatronix R8051XC related Virtual Registers**

The table below lists additional virtual registers ([VTR](http://www.keil.com/support/man/docs/uv3/uv3_db_exp_periphlvar.htm)), their size, range, default value and their meaning for the simulation.

| VTR | Size | Range | Default Value | Description |
| --- | --- | --- | --- | --- |
| RTC\_CLK | 32 Bit |  | 32768 Hz | External Clock for RTC |
| RTC\_SUBSEC | 8 Bit | 0 - 255 | 0 | RTC Subsecond counter |
| RTC\_SEC | 8 Bit | 0 - 59 | 0 | RTC Second counter |
| RTC\_MIN | 8 Bit | 0 - 59 | 0 | RTC Minute counter |
| RTC\_HOUR | 8 Bit | 0 - 23 | 0 | RTC Hour counter |
| RTC\_DOW | 8 Bit | 0 - 7 | 0 | RTC Day of Week counter (0: off; 1 - 7: Monday - Sunday) |
| RTC\_DAY | 16 Bit | 0 - 65536 | 0 | RTC Day counter |
| RTC\_RESET | 8 Bit | 0 - 1 | 0 | Writing 1 to RTC\_RESET causes a RTC reset |

## Example Programs

Example programs in the folder **..\C51\EXAMPLES\R8051XC** demonstrate some features of the Evatronix R8051XC core. All programs can be fully simulated with the uVision Debugger.

## Technical Support

At Keil Software, we are dedicated to providing you with the best development tools and technical support. That's why we offer numerous ways you can get the technical support you need to complete your embedded projects.

* [**Technical Support Knowledgebase**](http://www.keil.com/support)  
  More than 1500 technical support questions and answers are available in the Support Solutions Knowledgebase. When a new question arises, it is added to the knowledgebase which is continuously published to the Web. This enables you to get technical support at times when our support staff is unavailable.
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* [**Example Programs and Files**](http://www.keil.com/download)  
  Utility programs, example code, and sample projects are regularly added to the Download File section of the web site.
* [**Discussion Forum**](http://www.keil.com/discuss)  
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Many of the features of our Technical Support Knowledgebase and Web Site are the results of your suggestions. If you have any ideas that will improve them, please [give us your feedback](http://www.keil.com/support/feedback.asp)!

## Contact Details

If you experience any problems or have any questions about this Application Note, contact one of our [distributors](http://www.keil.com/distis) or offices for assistance.

| **In the USA...**  **KEIL - An ARM Company**  1501 10th Street, Suite 110  Plano, TX  75074  USA  800-348-8051 - Sales  972-312-1107 - Support  972-312-1159 - Fax  [sales.us@keil.com](mailto:sales.us@keil.com) - Sales E-Mail  [support.us@keil.com](mailto:E-Mailsupport.us@keil.com) - Support E-mail |  | **In Europe...**  **KEIL - An ARM Company**  Bretonischer Ring 16  D-85630 Grasbrunn  Germany  +49 89 456040-0 - Sales  +49 89 456040-24 - Support  +49 89 468162 - Fax  [sales.intl@keil.com](mailto:sales.intl@keil.com) - Sales E-Mail  [support.intl@keil.com](mailto:E-Mailsupport.intl@keil.com) - Support E-Mail |
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